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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/966,391	Applicant(s) DEMONE, PAUL W.	
	Examiner Minh Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's amendment filed on 7/14/03 has been received and entered. Claims 21-34 are pending. In view of the newly discovered prior art, the allowable subject matter indicated in the previous Office Action which is now incorporated to claim 23 is withdrawn. New grounds of rejections are set forth below. This action is NON-FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: -- Cascaded Charge Pump Power Supply With Different Gate Oxide Thickness Transistors --.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the latch, the intermediate latch outputs, the complementary latch outputs, the clock output driving stages and the structural relationships between these elements are not seen in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 29 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Due to the antecedent basis problems noted above, the claim fails to particularly point out the subject matters recited in the claim which are the latch, the intermediate latch outputs, the complementary latch outputs, the clock output driving stages. In other words, reading the specification, the Examiner cannot identify which elements and structures corresponding to these recited elements. It is suggested that the specification be amended to describe which elements and structures shown in the drawings corresponding to these recited elements. It is further notes that the recitation that a latch having intermediate latch outputs and complementary latch outputs appears misdescriptive because a latch has only two outputs.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,097,161, issued to Takano et al. in view of US Patent No. 5,006,974, issued to Kazerounian et al.

As per claim 21, Takano discloses a charge pump (Fig. 3), comprising:

a first (23-1) and second (23-2) pump cascades coupled in parallel (as shown) to an output node (HVOUT), each pump cascade having a plurality of pump stages coupled in series (for example, 23-1 pump cascade has T1, T2, … stages in series), the output node HVOUT receives the charges from the first and second pump cascades for providing the output supply voltage HVOUT greater than the power supply voltage (because this is the charge pump circuit); and

each pump stage has a FET configured as a diode and a FET configured as a capacitor (for example N1 is FET and C1 is FET, respectively).

Takano does not explicitly disclose the second oxide thickness of FETs in the last pump stages being greater than the first oxide thickness of FETs in the first pump stages as called for in the claim.

Kazerounian teaches charge pump stage circuit and in column 4, lines 39-45, he *explicitly* teaches in a charge pump circuit having a plurality of stages in series, the FETs in the first stage are not exposed to the high voltage as the FETs in the last stage, therefore, FETs in the last stage must be able to withstand high voltage than the first stage, i.e., the gate oxide insulation thickness of FETs in the last stage should be greater than the gate oxide insulation thickness of FETs in the first stage. In other words, the gate oxide insulation thickness of FETs in the last stage must be made thicker than the gate oxide insulation thickness of FETs in the first stage.

It would have been obvious to one skilled in the art at the invention was made to select FETs in the last stages can withstand a higher voltage than FETs in the first stages in the Takano charge pump circuit to prevent breakdown.

The motivation and/or suggestion for doing so would have been obvious, i.e., ensure the Takano charge pump circuit does not breakdown when operating in a high voltage environment.

As per claim 22, (2n)th pump stage in the first pump cascade (23-1) receives a first clock signal and (2n+l)th pump stage receives a second clock signal, n being an integer greater than or equal to zero (met since capacitors C2, C4, … receive the first clock signal (a) and capacitors C1, C3, …receive the second clock signal (b)); and

(2n)th pump stage of the second pump cascade (23-2) receives the second clock signal and (2n +1)th pump stage receives the first clock signal, n being an integer greater than or equal to zero (met since capacitors C2, C4, … receive the second clock signal (b) and capacitors C1, C3, … receives the first clock signal (a)).

As per claim 23, C1, N1, … in both of the pump cascades are PFETs.

As per claim 24, N1 and C1 coupled to ground.

As per claim 25, the recited diode reads on Tn.

As per claim 26, Tn is a FET, and since the diode Tn is located in the last stage, the gate oxide thickness should be the gate oxide of the second oxide thickness.

As per claim 27, see Fig. 4, the a and b signals are non-overlapping.

As per claim 28, the recited system clock signal reads on one of the signals ((a-1), (a-2), (b-1), (b-2)) which is used to control (generate) the a and b clock signals, the limitation the charge pump stages pump charge in response to the rising and falling edge is merely the operation of the charge pump when driving by clock signals a and b.

As per claim 29, due to the indefiniteness problems noted above, patentability of this claim cannot be positively determined in this Office Action, it appears that the recited limitations read on the control circuit 3, switching switches I1, …, I4 and circuits 22-1, 22-2.

As per claims 30-34, the claims are rejected for the same reasons as claims 21-23, 26 and 27, respectively.

Response to Arguments

6. No arguments is provided.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 6,473,321, issued to Kishimoto also explicitly teaches the key point of this invention, i.e., the oxide thickness of the FETs are different in stages (column 4, lines 42-54).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

9/12/03

Minh Nguyen
Primary Examiner
Art Unit 2816